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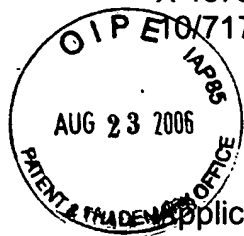
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application / Conf. No.	10/717,359 / 8181
	Filing Date	November 18, 2003
	First Named Inventor	Sudip K. Nag
	Examiner Name	Vuthe Siek
	Art Unit	2825
	Patent No.	
	Attorney Docket Number	X-1376 US
Express Mail Receipt No.		
Total Number of Pages in This Submission		

ENCLOSURES (check all that apply)		
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X-1376 US
10/717,359

PATENT
Conf. No.: 8181

IN THE UNITED STATES PATENT OFFICE

Applicant: Sudip K. Nag
Assignee: Xilinx, Inc.
Title: Method and Apparatus for Timing Characterization of Integrated Circuit Designs
Serial No.: 10/717,359 File Date: 11/18/2003
Examiner: Vuthe Siek Art Unit: 2825
Docket No.: X-1376 US Conf. No.: 8181

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RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

In response to the Final Office Action mailed from the Patent Office on July 13, 2006, Applicant makes the following remarks.

A listing of claims begins on page 2 of this paper.

Remarks begin on page 6 of this paper.